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Gwent NP9 1RH

1. Your reference

N.77197 MN

2. Patent application number

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9916060.8

08 JUL 1999

3. Full name, address and postcode of the or of each applicant (underline all surnames)

ISIS INNOVATION LIMITED
2 South Parks Road,
Oxford,
OX1 3UB

Patents ADP number (if you know it)

UK

If the applicant is a corporate body, give the country/state of its incorporation

3998564001

4. Title of the invention

Printed circuit fabrication

5. Name of your agent (if you have one)

J A KEMP & CO

"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode)

14 SOUTH SQUARE
GRAY'S INN
LONDON WC1R 5LX

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Country

Priority application number
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Date of filing
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Number of earlier application

Date of filing
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Description	5
Claim(s)	3
Abstract	1
Drawing(s)	2

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Translations of priority documents

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Request for preliminary examination and search (*Patents Form 9/77*) 1

Request for substantive examination (*Patents Form 10/77*)

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11. I/We request the grant of a patent on the basis of this application

Signature J. A. Kenley Date 8 July 1999

12. Name and daytime telephone number of person to contact in the United Kingdom M. J. Nicholls
0171 405 3292

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PRINTED CIRCUIT FABRICATION

The present invention relates to the fabrication of printed circuits and in particular to methods of producing such printed circuits by etching a desired conductor pattern into a layer of conductive material on a substrate.

Printed circuit boards which consist of a pattern of conductive material, usually copper, on a substrate, such as a resin board, are well known and widely used in the electronics industry. Conventional methods for producing such printed circuits involve the preparation of a uniform layer of conductive material, usually copper, on a support, such as the resin board (though flexible supports are increasingly being used), the desired conductor pattern then being etched into the conductive material. This etching process involves first putting a mask of resist in the desired pattern on the conductive material and then spraying the conductive layer with an etchant to remove those areas of the conductor which are not masked by the resist. The pattern of resist is conventionally produced by laying down a uniform layer of photo resist, which is then exposed to a pattern of UV light corresponding to the desired circuit pattern (or its negative). Areas of the resist which have been exposed (or not exposed in the negative process) are then dissolved away. Usually the pattern of UV light is created by using a mask, or photographic master, which itself is in the pattern of the desired printed circuit or its negative. Such masks can be produced by various techniques such as laser plotting or conventional photography.

With the miniaturisation of electronic devices printed circuits of finer and finer resolution are required all the time. At the moment printed circuits having a fine resolution include conductors of widths as narrow as 150 microns. However, there is a need for printed circuits with conductors much narrower than this, down to 30 microns or below, even in the range 10 to 12 microns. A problem with producing such fine circuits is that the circuits often contain imperfections, such as the narrowest conductors being of varying width, or even broken. This places limits on the fineness of the resolution which can be achieved.

The present invention provides an improved method for producing printed

circuit boards in which the problems associated with producing very narrow conductor elements when etching a printed circuit are reduced. In particular the present invention proposes that the conductor elements of the circuit should be delineated by etched regions of constant width. In other words, they should be separated from regions of unused conductor by a constant width etch band. This means that, as compared with a conventional printed circuit, there will be large areas of unused conductor (e.g. copper) left on the circuit board. Conventionally all such unused areas would be etched away. However with the present invention they are left on the printed circuit board, and just separated from the conductors by the constant width etch bond.

Thus the present invention involves a modification to the method of producing the mask which is used to define the resist pattern for the etching process. The mask is designed so that the desired printed circuit pattern is delineated by a constant width etch band.

The etch band is preferably of the same width of the narrowest conductor separation or conductor in the printed circuit. It is particularly useful where the printed circuit conductor pattern includes conductor regions less than about 30 microns wide or spaced by less than about 30 microns.

With the present invention the same amount of conductor needs to be etched away along all conductor elements. With a conventional printed circuit board some areas where the conductors are very closely spaced will require less copper to be etched away than areas where there are very few conductors, or whether conductors are widely spaced. It is this difference in the amount of conductor which needs to be etched away which causes variations in etch rate. The local etch rate varies according to the amount of local conductor which has to be etched away. Because with the present invention the amount of local conductor which has to be etched away is constant (because it consists of a constant width etch band delineating the conductors) the etch rate is the same over the whole pattern. Thus the width of the conductors which are produced is relatively constant and problems of undue narrowing of conductors, undercutting of conductors by etchant, and breaking of conductors are reduced.

The invention will be further described by way of non-limitative example with reference to the accompanying drawings in which:-

Figure 1 illustrates schematically a conventional printed circuit pattern;

Figure 2 illustrates the corresponding pattern according to the present invention; and

Figure 3 illustrates at a magnified scale an actual mask produced by an embodiment of the present invention.

Figure 1 shows schematically a very simply printed circuit which the present invention can be applied. Figure 1 illustrates the circuit in conventional form and figure 2 illustrates the modification according to the invention. As can be seen in figure 1 the printed circuit is defined on a substrate 1 and consists of a set of parallel conductors 3a, 3b and 9 of which the conductors 3a and 3b lead to contact pads 5 and the conductor 9 leads off to another region of the printed circuit. It can be seen that the spacing between the conductors varies across the pattern, it being narrow in regions 6 where the conductors are parallel and closely spaced, while being wider in regions 7 and 11 near the contact pads and the edge of the printed circuit. It can also be seen that the conductor 3a has on one side a very narrow spacing to the neighbouring conductor 3b and on the other side a very wide area where all conductor has been etched away. Similarly the conductor 9 has, in region 11, areas on both sides where much conductor has been etched away. Where this pattern is produced at fine resolutions, such as the conductors being of 30 microns width or less, e.g. 10 to 12 microns, it is found that the width of the conductors produced varies in the different regions 6, 7 and 11. The etch rate would be lower in the regions 6 compared to the widely spaced regions 7 and 11. Thus given a constant etching time, the conductors would narrow (because of increased etching) in the regions approaching the contact pads or where the conductor extends to other parts of the printed circuit as at 11.

The present invention solves this problem by modifying the pattern of conductor which is produced in the etching process. The result of this modification is illustrated in figure 2. It can be seen that each of the conductor elements is now surrounded by a constant width etch band 20. The conductor elements are therefore

separated from unused regions of conductor 22 by this constant width band. Thus the amount conductive material which needs to be etched away is now constant over the whole area of the illustrated pattern. This means that the etch rate will be the same over the whole pattern, and variations in width of the conductors produced will be much smaller.

Of course although figure 2 illustrates that only the constant width etch band 20 is etched away, it may be that there are remote regions of the printed circuit substrate which can be etched away without affecting the etch rate locally around the conductors. The invention is concerned with producing a constant etch rate around the conductor elements. Thus given a printed circuit product it may be that only certain regions need to include the constant width etch band delineating the conductors. Edge regions or regions which do not include fine conductors may be produced in a conventional way.

It will be appreciated that in a region where the conductors consist of parallel closely spaced elements, to enable the etch rates to be the same as the etch rate between such elements, the etch band must be of the same width as the spacing between the conductor elements. Often a constant mark-to-space ratio is used which means that the etch band can be of the same width as the narrowest conductor on the board.

Figure 3 is a magnified view of an actual mask designed according to an embodiment of the invention. The white areas correspond to areas of conductor which will be left on the printed circuit. Thus there are a plurality of contact pads 5 which are connected by conductor elements or "wires" 3 to another row of contact pads 4. In addition to these conductor elements it can be seen that there are large areas of unused conductor 15 which are left because the conductor pattern is delineated by the constant width etch band 10. The constant width etch band is of the same width of the separation between the conductors in the region 17 where they are narrowly spaced.

While the present invention has been described as being applied in the design of the mask for using the etching process, it will of course be appreciated that it can be applied however the selective etching of conductor is achieved. Thus, for

instance, it may be that the uniform layer of resist is illuminated in a scanning process, rather than by using a mask, or is written directly by a light beam.

Alternatively the resist pattern may be produced by other means. However the present invention is still applicable in that the pattern of resist must define a constant
5 width etch band delineating the desired conductor regions in the pattern.

CLAIMS

1. A method of producing a mask for use in producing a resist pattern for etching of a printed circuit, comprising defining in the mask a constant width etch band delineating the desired printed circuit conductor pattern.

2. A method according to claim 1 wherein the etch band is of substantially the same width as the narrowest conductor or the narrowest separation between conductors in the printed circuit.

3. A method according to claim 1 wherein the etch band separates the desired printed circuit conductor pattern from regions of unused conductor on the printed circuit.

4. A method according to claim 1, 2 or 3 wherein the printed circuit conductor pattern includes conductor regions less than about 30 microns wide.

5. A method according to claim 1, 2, 3 or 4 wherein the printed circuit conductor pattern includes conductor regions spaced by less than about 30 microns.

6. A method according to any one of the preceding claims wherein the etch band is less than about 30 microns wide.

7. A mask for use in producing a resist pattern for etching of a printed circuit, the mask being produced by the method of any one of the preceding claims.

8. A printed circuit in which the printed circuit elements are delineated by a constant width etch band.

9. A printed circuit according to claim 8 in which the etch band separates

the printed circuit elements from regions of unused conductor.

10. A printed circuit according to claim 8 or 9 wherein the etch band is of substantially the same width as the narrowest conductor or the narrowest separation
5 between conductors in the printed circuit.

11. A printed circuit according to claim 8, 9 or 10 wherein the printed circuit conductor pattern includes conductor regions less than about 30 microns wide.

10 12. A printed circuit according to claim 8, 9, 10 or 11 wherein the printed circuit conductor pattern includes conductor regions spaced by less than about 30 microns.

15 13. A printed circuit according to any one of claims 8 to 12 wherein the etch band is less than 30 microns wide.

20 14. A method of producing a printed circuit comprising a pattern of conductor elements, the method comprising the steps of: defining on a printed circuit substrate a pattern of resist to leave exposed regions of conductor to be etched away, the exposed regions comprising areas of constant width delineating the conductor elements.

25 15. A method according to claim 14 wherein the conductor elements include elements less than about 30 microns wide.

16. A method according to claim 14 or 15 wherein the pattern includes conductor elements spaced by less than about 30 microns.

30 17. A method according to claim 14, 15 or 16 wherein the regions of constant width are of substantially the same width as the narrowest element or narrowest separation between elements in the printed circuit.

18. A mask or a printed circuit substantially as hereinbefore described with reference to and as illustrated in figures 1 and 3 of the accompanying drawings.

19. A method of producing a mask or a printed circuit substantially as
5 hereinbefore described.

ABSTRACT
PRINTED CIRCUIT FABRICATION

5 A mask for producing a printed circuit board is defined in which the
conductor elements of the printed circuit pattern are delineated by a constant width
etch band. This means that all conductors are separated from neighbouring areas of
conductive material by the same distance. Thus etch rates across the printed circuit
pattern do not vary according to the separation of the conductors.

10

Figure 2

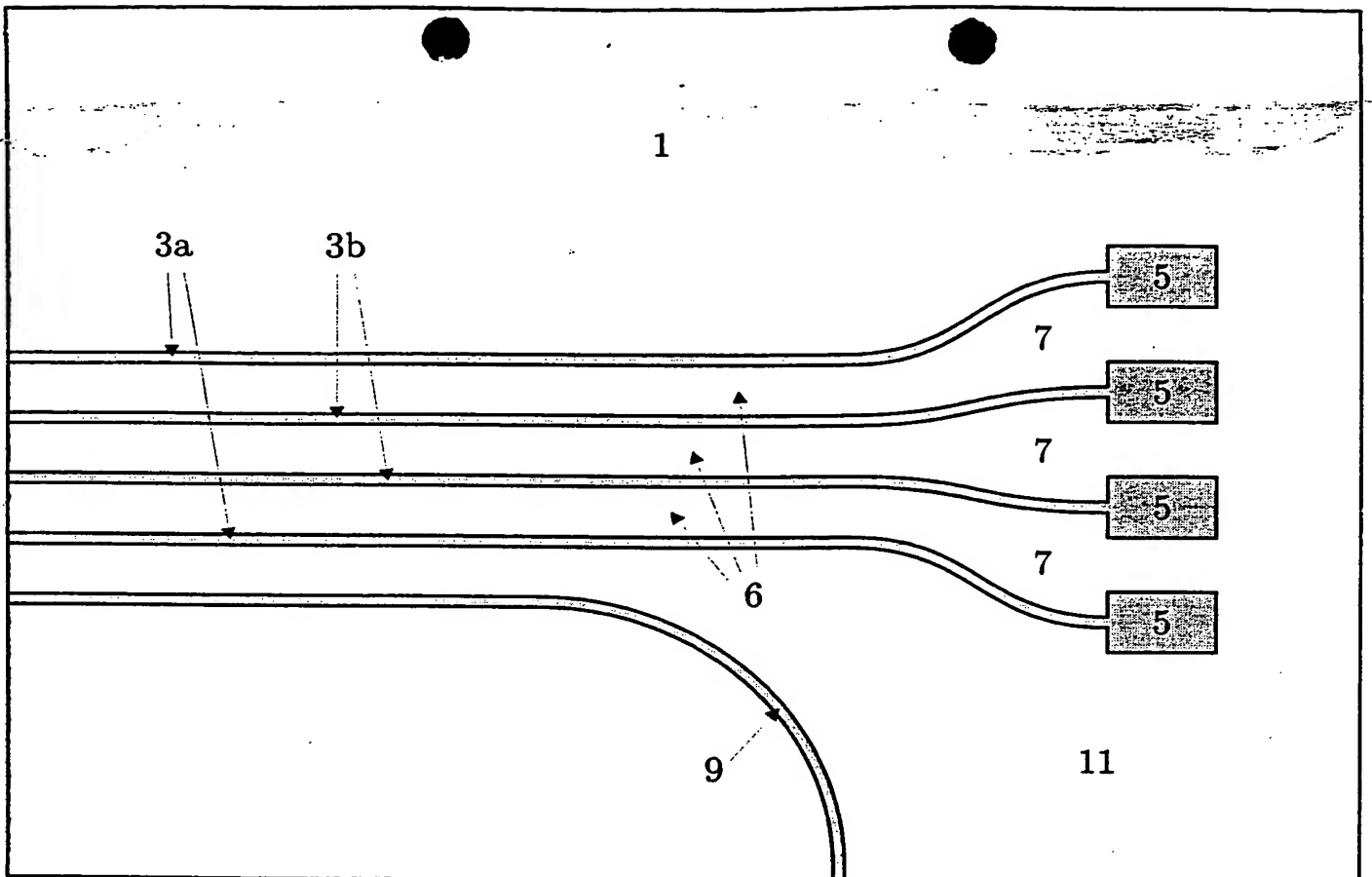


Fig. 1

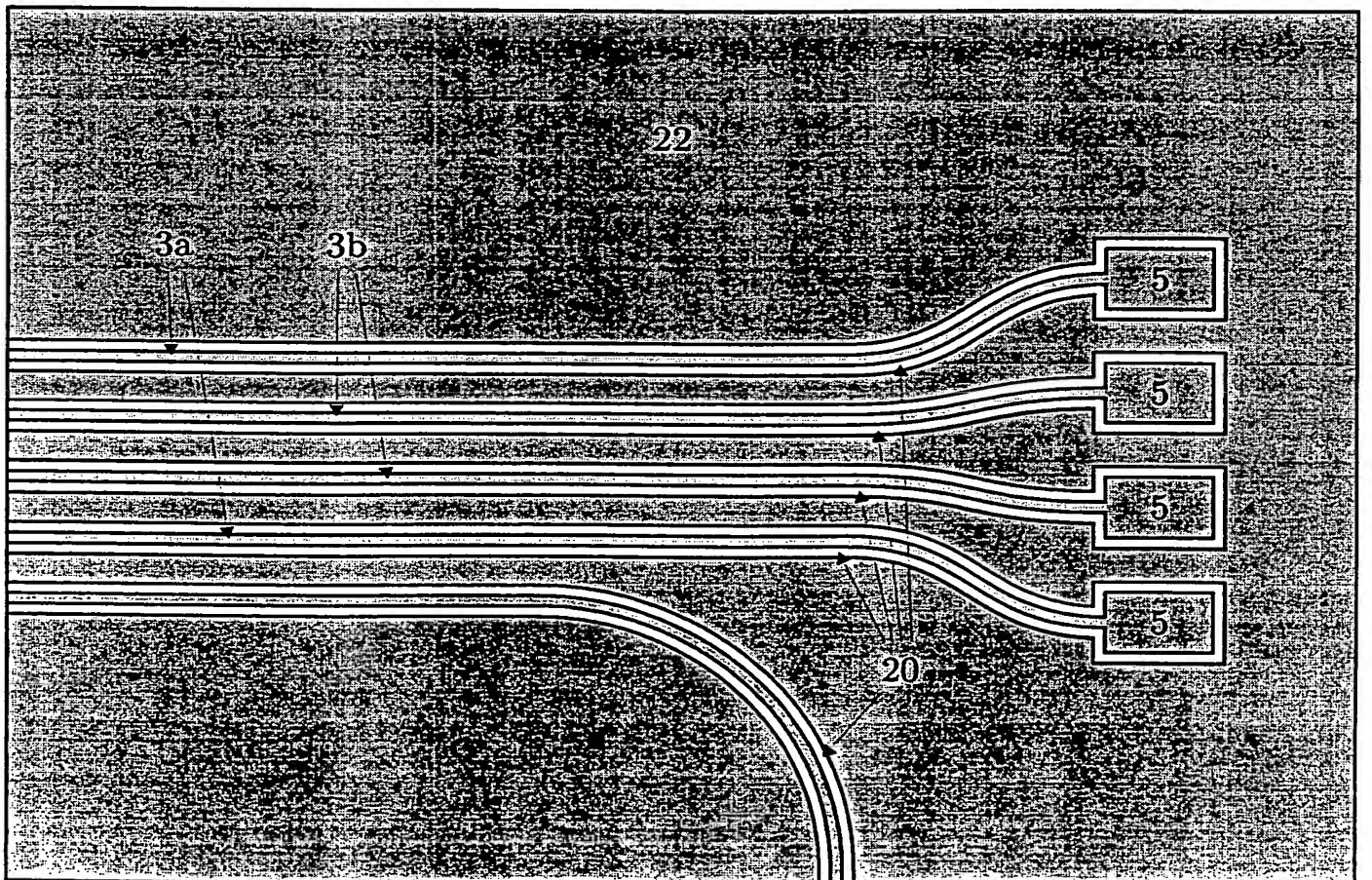


Fig. 2

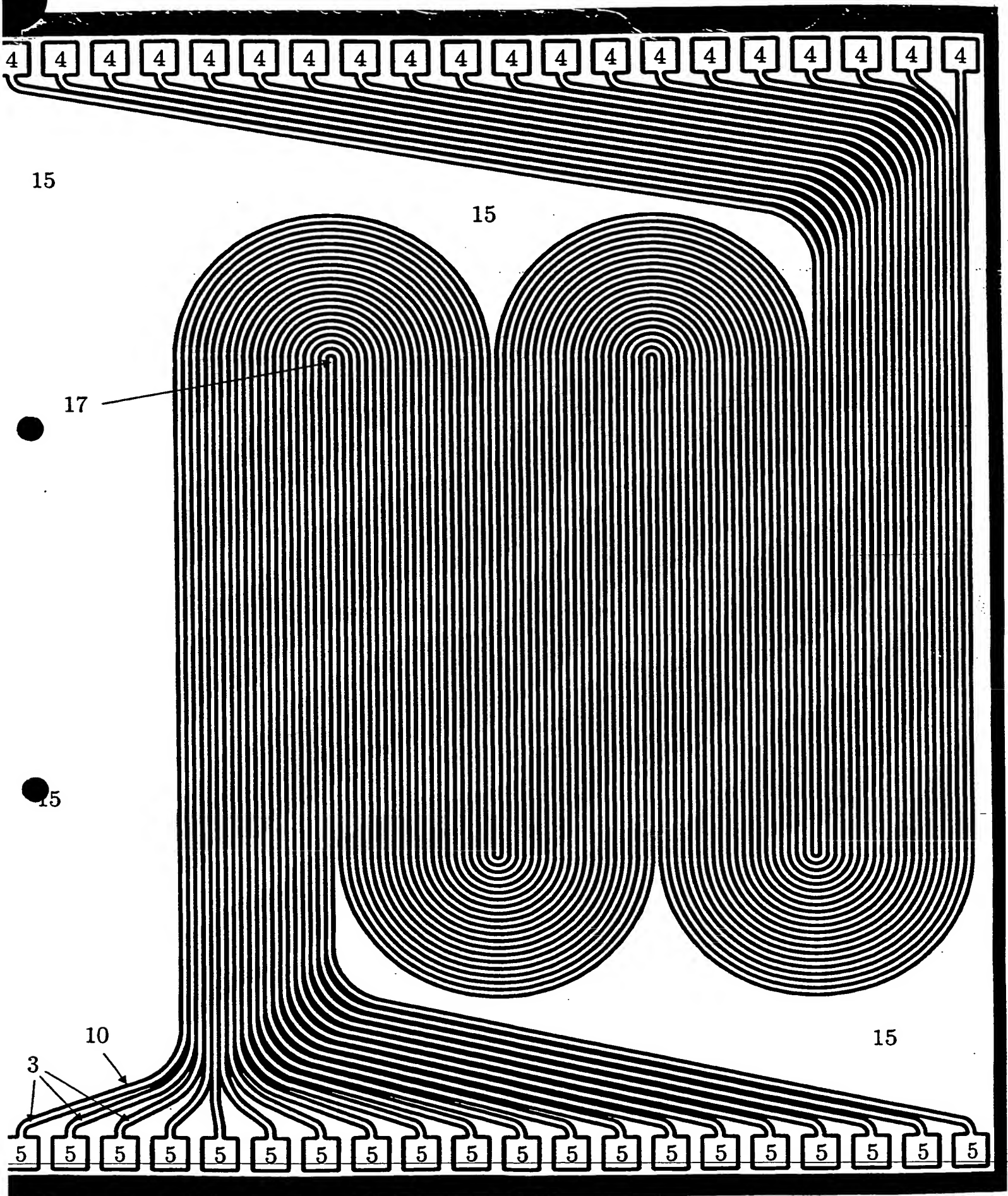


Fig. 3

